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UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Wen-mei Hwu et al.**	Atty. Docket No. 042302-0269900 ITI-001(U)
Serial No.: **09/728,441** Filed: **December 1, 2000**	Examiner: Aimee J. Li Art Unit: 2183
For: **Method And Apparatus For Modulo Scheduled Loop Execution In A Processor Architecture**	

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Date of Deposit: June 30, 2004

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INFORMATION DISCLOSURE STATEMENT
1.97(c)(2)

Enclosed is Form PT-1449 along with the listed references.

The filing of this information disclosure statement shall not be construed as a representation that a search has been made (37 CFR 1.97(g)), nor as an admission that the information cited is, or is considered to be, material to patentability, nor an admission that no other material information exists. The filing of this information disclosure statement shall not be construed as an admission against interest in any manner. Notice of January 9, 1992, 1135 O.G. 13-25, at 25.

This submission is made before the mailing date of a final office action or a notice of allowance. The Commissioner is authorized to charge deposit account 50-2213 (Order No. 042302-0269900) for the $180.00 fee required by 37 CFR § 1.17(p)

Respectfully submitted
PILLSBURY WINTHROP LLP

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INFORMATION DISCLOSURE CITATION PTO-1449	Atty Docket 042302-0269900	Serial No. 09/728,441
	Applicant : Hwu et al.	
Date Mailed: June 30, 2004	Filing Date: December 1, 2000	Group Art Unit: 2183

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation Yes	Translation No

	B. R. Rau and C. D. Glaeser, Some Scheduling Techniques and An Easily Schedulable Horizonal Architecture for High Performance Scientific Computing,in *Proceedings of the 20th Annual Workshop on Microprogramming and Microarchitecture*, pp. 183-198, October 1981
	J. C. Dehnert, P. Y. Hsu, and J. P Bratt, Overlapped Loop Support in the Cydra 5,in *Proceedings of the 3rd International Conference on Architectural Support for Programming Languages and Operating Systems*, pp. 26-38, April 1989.
✓	TMS320C6000 CPU and Instruction Set Reference Guide,Tech. Rep. SPRU189F, Texas Instruments, Oct. 2000, Chapters 1 and 2.
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	B. R. Rau, M. S. Schlansker, and P. Tirumalai, Code generation schemas for modulo scheduled do-loops and while-loops,Tech. Rep. HPL-92-47, Hewlett Packard Labs, April 1992
	D. M. Lavery, *Modulo Scheduling for Control-Intensive General-Purpose Programs*. Ph.D. thesis, Department of Electrical and Computer Engineering, University of Illinois, Urbana, IL, 1997

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.